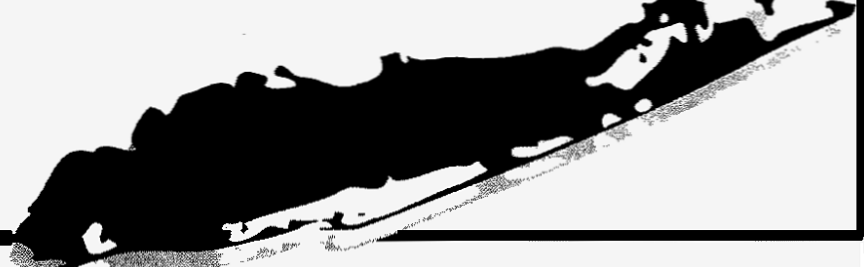




The Materials Information Society

LONG ISLAND CHAPTER

METALLAGRAM



Volume 61 Issue 6

Chapter website: <http://DoL1.eng.sunysb.edu/asm/>

PAST CHAIRS NIGHT

Next Meeting Wednesday, February 19, 2020

Where Pollo Rico Latin Bistro, Centereach, NY

Topic: Semiconductor Logic Transistor Contact Optimization using Process Explorer Simulation

Speaker: Dr. Anthony Lee, Farmingdale SU

Social hour ... 6:00 pm Dinner ... 7:00 pm Meeting ... 8:00 pm

Members ... \$25 Guests ... \$27 Students ... \$15

(New and recently transferred-in members free)

Reservations appreciated – call Peter Indrigo at 631-589-6666

WELCOME TO THE CHAPTER!

Gary Chawla, Axim Micro Sabrina Hernandez, East Patchogue

All new members, including those who have transferred in from another Chapter, are invited to dine free at a regular meeting of their choice. Please take us up on this offer - come along to the meeting and introduce yourself. This is an excellent way to meet with other Chapter members and to establish new business and social relationships in the area.

The Speaker

Dr. Anthony Lee obtained his BS degree in Metallurgical Engineering from Seoul National University. He attended Stanford University for his graduate study in Materials Science and Engineering. In Stanford, his Ph.D. research was focused on Negative Electron Affinity III-V Photocathode Device in the application of Night Visions. He was also a member of Stanford Synchrotron Radiation Laboratory as a part of Stanford Linear Accelerator Center funded and operated by Department of Energy. He was an employee of IBM and Global Foundries working on Semiconductor Process Integration and Development. Lately he joined Farmingdale State College as an Assistant Professor of Mechanical Engineering Technology. His latest research interest is focused on Transistor Process Exploration.

The Topic

Today's Semiconductor Transistor Scaling has followed the Moore's law consistently, yet the challenges of meeting twice density in two years become more demanding. The fabrication time to process a bare wafer to the complete transistor contact shape formation consumes more than two months due to the extreme complexity of process steps. Incoming FINFET lithographic steps play a role to generate an outcome contact area and orientation: Gate lithography (PC), FIN lithography (RB, RC). The linearity and correlation between one of incoming lithography layer and the resulting contact layer lines up with the expectation, the less overlay shift the more contact area formation, while multiple factors are often convoluted. Process Explorer is a 3D large-area scale process simulation. It is lately developed and differs from the traditional device simulation tool: (1) as long as the layout is prepared, the large area generation is possible. (2) process steps are sophisticated using accurate meshing and feedback loop. (3) the output data is transferrable to device simulation softwares further continuing on electrical data generation. After the introduction and brief summary on the result, there is a parallel study of Resistive Random Memory (ReRAM) device experimental data to present briefly to explain the difference between simulation and experimental method.



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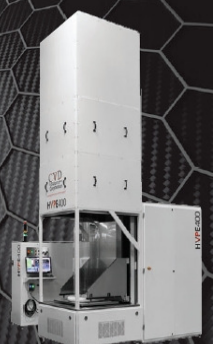
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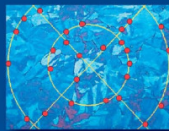
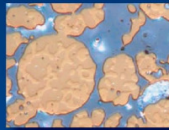
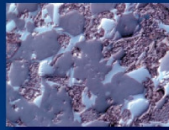
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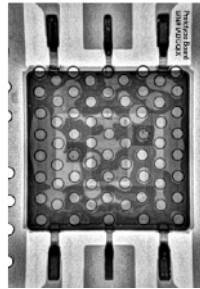
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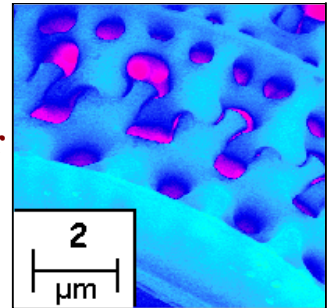
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Long Island Chapter Meeting Schedule

Mar. 25, 2020 Sustaining Members Night
 Speaker: Don Weidner, SBU
 Topic: Characterization of High Pressure Metals and Oxides
 Place Pollo Rico, Centereach

Apr. 22, 2020 Student Night
 Various speakers, posters

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Feb. 2020 – no meeting